Location	Device/Block	Address	Area Size	Access Size	Notes	Possible DMA	Access Time (clock:100MHz) read 1byte	read 2byte	read 4byte	read 32byte	write 1byte	write 2byte	write 4byte	write 32byte	Access times are simulation optimums. (More time is required in the event of access contentions.)
CPU Bus	System Memory [SDRAM]	0C00 0000 – 0CFF FFFF (image) 0E00 0000 – 0EFF FFFF	16Mbyte	1/2/4/32byte(RD/WR)	Access is inhibited until the CPU BSC is set.	All DMA	7or12	7or12	7or12	7or12	4or9	4or9	4or9	4or9	Row hit :RD= 7/WR=4 Row miss:RD=12/WR=9
G1 Bus	System ROM [Mask ROM]	0000 0000 – 001F FFFF	2Mbyte	1/2/4/32byte(RD/–)	Access is restricted to System ROM until the CPU BSC is set. 32-byte access is inhibited until G1RRC and G1RWC are set. No image appears in 02000000-021FFFFF.	CPU-ch1/ch3	44	63	99	618					G1RRC = 00000400 G1RWC = 00000400
	Flash Memory [Flash Memory]	0020 0000 – 0021 FFFF	128Kbyte	1/2/4/32byte(RD) 1 byte(WR)	Access is inhibited until G1FRC and G1FWC are set. The number of writes is limited, and special sequence and time management are required. No image appears in 02200000-0221FFFF.	CPU-ch1/ch3	41	55	83	489	28				G1FRC = 00000200 G1FWC = 00000200
	GD-ROM	005F 7000 – 005F 70FF (image) 025F 7000 – 025F 70FF	256byte	1/2 byte(RD/WR)	GD-ROM drive (PIO access). Access is inhibited until G1CRC and G1CWC are set. Access size varies according to register.	GD-DMA	39	39			28	28			G1CRC = 00000222 G1CWC = 00000222
G2 Bus	MODEM	0060 0000 – 0060 07FF (image) 0260 0000 – 0260 07FF	2Kbyte	1 byte(RD/WR)	An internal MODEM register. A special sequence is required for access.	None	67				44				
	G2 External Area	0100 0000 – 01FF FFFF 0300 0000 – 03FF FFFF 1400 0000 – 17FF FFFF	16Mbyte 16Mbyte 64Mbyte	1/2/4/32byte(RD/WR)	External expansion area. Access size depends on the connected hardware.	CPU-ch1/ch3 GD-DMA Ext-DMA1,Ext-DMA2,Dev-DMA	56	56	60	84	28	28	28	52	Access times for a zero wait virtual device.
in AICA	AICA Sound Control Register	0070 0000 – 0070 7FFF (image) 0270 0000 – 0270 7FFF	32Kbyte	4 byte(RD/WR)	Register for AICA internal sound control.	None			?				?		
	AICA RTC Control Register	0071 0000 – 0071 0007 (image) 0271 0000 – 0271 0007	8byte	4 byte(RD/WR)	Register for the AICA internal Real Time Clock.										
AICA Local Bus	AICA Wave Memory [SDRAM]	0080 0000 – 009F FFFF (image) 0280 0000 – 029F FFFF	2Mbyte	4 byte(RD/WR)	Memory for AICA sound.	GD-DMA AICA-DMA			?				?		
Holly Local Bus	Texture Memory (PVR I/F) 64bit Access ※8	0400 0000 – 047F FFFF (image) 0600 0000 – 067F FFFF	8Mbyte	2/4/32byte(RD/WR)	Texture Memory access (64bit mode) through Root Bus.	CPU-ch1/ch3 GD-DMA,PVR-DMA,AICA-DMA		41	41	61		12	12	38	
	Texture Memory (PVR I/F) 32bit Access ※8	0500 0000 – 057F FFFF (image) 0700 0000 – 077F FFFF	8Mbyte	2/4/32byte(RD/WR)	Texture Memory access (32bit mode) through Root Bus.	Ext-DMA1,Ext-DMA2,Dev-DMA		41	41	61		12	12	38	
	Polygon Converter (TA FIFO) ※h	1000 0000 – 107F FFFF (image) 1200 0000 – 127F FFFF	8Mbyte	32byte(–/WR)	A polygon parameter converter (through TA FIFO) Confirmation that FIFO has been emptied is required when writing to the CPU. Ch2-DMA and Sort-DMA are not possible concurrently.	ch2-DMA,Sort-DMA								?	
	YUV Converter (TA FIFO) ※送	1080 0000 – 10FF FFFF (image) 1280 0000 – 12FF FFFF	8Mbyte	32byte(–/WR)	YUV converter (through TA FIFO). Confirmation that FIFO has been emptied is required when writing to the CPU. Ch2-DMA and Sort-DMA are not possible concurrently.	ch2-DMA								858 984	Clock cycles required for YUV420 when data to be transferred is 3072 bytes. Clock cycles required for YUV422 when data to be transferred is 3072 bytes.
	Texture Memory (TA FIFO) 32/64bit WR ※4	1100 0000 – 117F FFFF (image) 1300 0000 – 137F FFFF	8Mbyte	32byte(–/WR)	Access through TA FIFO Texture Memory. 32bit/64bit mode selection is possible using LMMODE0,1. Confirmation that FIFO has been emptied is required when writing to the CPU. Ch2-DMA and Sort-DMA are not possible concurrently.									5 8	64bit Access 32bit Access
in Holly	System Control Register	005F 6800 – 005F 69FF (image) 025F 6800 – 025F 69FF	512byte	4 byte(RD/WR)	System control register used by the interrupt controller, etc.	None			5				5		
	Maple I/F Control Register	005F 6C00 – 005F 6CFF (image) 025F 6C00 – 025F 6CFF	256byte	4 byte(RD/WR)	Control register for the Maple I/F block.				22				12		
	G1 I/F Control Register	005F 7400 – 005F 74FF (image) 025F 7400 – 025F 74FF	256byte	4 byte(RD/WR)	Control register for the G1 I/F block.				24				12		
	G2 I/F Control Register	005F 7800 – 005F 78FF (image) 025F 7800 – 025F 78FF	256byte	4 byte(RD/WR)	Control register for the G2 I/F block.				38				12		
	PVR I/F Control Register	005F 7C00 – 005F 7CFF (image) 025F 7C00 – 025F 7CFF	256byte	4 byte(RD/WR)	Control register for the PVR I/F block.				24				12		
	TA/PVR Core Control Register	005F 8000 – 005F 81FF (image) 025F 8000 – 025F 81FF	512byte	4 byte(RD/WR)	Control register for TA and PVR Core.				34				14		
	FOG Table	005F 8200 – 005F 83FF (image) 025F 8200 – 025F 83FF	512byte	4/32byte(RD/WR)	Holly internal RAM. Only the lower 16 bits are valid.	CPU-ch1/ch3,PVR-DMA			34	?			14	?	
	Palette RAM	005F 9000 – 005F 9FFF (image) 025F 9000 – 025F 9FFF	4Kbyte	4/32byte(RD/WR)	Holly internal RAM.	CPU-ch1/ch3,PVR-DMA			34	?			14	?	

＊Texture Memory contains 8Mbyte, but the access method depends on the address.
Apparent memory organization differs with 64bit and 32bit access.

Pass	Block	DMAC	Source	Destination	CPU DMAC ch Used	Transfer Capacity (MByte/sec)	
TA FIFO	DDT I/F	ch2-DMA	System Memory	Polygon Converter (TA FIFO)	ch2	?	
				YUV Converter (TA FIFO)		291.8	YUV420
						349.4	YUV422
				Texture Memory (TA FIFO)		702.6	64bitAccess
						364.7	32bitAccess
		Sort-DMA	System Memory	Polygon Converter (TA FIFO)	ch0	?	
RootBus	G1 I/F	GD-DMA	GD-ROM	System Memory		14.4	
				Texture Memory (PVR I/F)		14.4	
				AICA Wave Memory		11.3	
				G2 External Area		14.4	
	G2 I/F	AICA-DMA	System Memory	AICA Wave Memory		11.3	
			Texture Memory (PVR I/F)			11.3	
		Ext-DMA1	G2 External Area	System Memory		26.0	
				Texture Memory (PVR I/F)		26.0	
			System Memory	G2 External Area		24.1	
			Texture Memory (PVR I/F)			23.9	
		Ext-DMA2	G2 External Area	System Memory		26.0	
				Texture Memory (PVR I/F)		26.0	
			System Memory	G2 External Area		24.1	
			Texture Memory (PVR I/F)			23.9	
	Maple I/F	Maple-DMA	System Memory	Maple Device		0.25	
			Maple Device	System Memory		0.25	
	PVR I/F	PVR-DMA	System Memory	FOG Table		?	
				Palette RAM		?	
				Texture Memory (PVR I/F)		64.3	64bitAccess
						64.3	32bitAccess
			FOG Table	System Memory		?	
			Palette RAM			?	
			Texture Memory (PVR I/F)			51.4	64bitAccess
						51.4	32bitAccess

＊ Transfer capacities are simulation optimums.

System Memory	0C00 0000 – 0CFF FFFF
	0E00 0000 – 0EFF FFFF(image)
G2 External Area	0100 0000 – 01FF FFFF
	0300 0000 – 03FF FFFF
	1400 0000 – 17FF FFFF
AICA Wave Memory	0080 0000 – 009F FFFF
	0280 0000 – 029F FFFF(image)
Texture Memory (PVR I/F) 64bit Access	0400 0000 – 047F FFFF
	0600 0000 – 067F FFFF(image)
Texture Memory (PVR I/F) 32bit Access	0500 0000 – 057F FFFF
	0700 0000 – 077F FFFF(image)
Polygon Converter (TA FIFO)	1000 0000 – 107F FFFF
	1200 0000 – 127F FFFF(image)
YUV Converter (TA FIFO)	1080 0000 – 10FF FFFF
	1280 0000 – 12FF FFFF(image)
Texture Memory (TA FIFO) 32/64bit WR	1100 0000 – 117F FFFF
	1300 0000 – 137F FFFF(image)
FOG Table	005F 8200 – 005F 83FF
	025F 8200 – 025F 83FF(image)
Palette RAM	005F 9000 – 005F 9FFF
	025F 9000 – 025F 9FFF(image)