Notes concerning Drawing System Registers

Register Name	Address	Notes and Explanations
REVISION	0x005F8004	Used in combination with SB_REVISION(0x005F689C) to give the following meanings: REVISION=0x01 SB_REVISION=0x01 CLX1.0 and CLX1.1 SB_REVISION=0x02 CLX1.5 and CLX1.6 REVISION=0x11 SB_REVISION=0x04 CLX2.0 SB_REVISION=0x05 CLX2.1 SB_REVISION=0x06 CLX2.05 and CLX2.06 SB_REVISION=0x08 CLX2.2 SB_REVISION=0x09 CLX2.3 SB_REVISION=0x0A CLX2.4 (product) Regard all combinations not shown above as CLX2.4 (product).
SOFTRESET	0x005F8008	bit0: TA soft reset Reset when launching TA. bit1: Pipeline soft reset Only to be used when drawing does not end for some reason. Drawing output cannot be assured if reset. bit2: SDRAM I/F soft reset Release only upon boot. The setting of this bit cannot be changed. When resetting, set only applicable bits to '1'.
TEST_SELECT	0x005F8018	Access inhibited.
PARAM_BASE	0x005F8020	Must not be rewritten while drawing is in progress.
REGION_BASE	0x005F802C	Must not be rewritten while drawing is in progress.
SPAN_SORT_CFG	0x005F8030	For products, set 0x00000101. No other values can be set.
VO_BORDER_COL	0x005F8040	When specifying white, set brightness to 75% or less (less than 0xC0). Setting higher values may cause image distortion or burn-in, depending on the TV.
FB_R_CTRL	0x005F8044	This register should only be written to when nothing is displayed. If rewritten when something is displayed, the image may be disrupted.
FB_W_CTRL	0x005F8048	Must not be rewritten while drawing is in progress.
FB_LINESTRIDE	0x005F804C	Must not be rewritten while drawing is in progress.
FB_R_SOF1	0x005F8050	Setting becomes valid immediately prior to display.
FB_R_SOF2	0x005F8054	Setting becomes valid immediately prior to display.
FB_R_SIZE	0x005F8044	This register should only be written to when nothing is displayed. If rewritten when something is displayed, the image may be disrupted.
FB_W_SOF1	0x005F8060	Must not be rewritten while drawing is in progress.
FB_W_SOF2	0x005F8064	Must not be rewritten while drawing is in progress.
FB_X_CLIP	0x005F8068	Must not be rewritten while drawing is in progress.
FB_Y_CLIP	0x005F806C	Must not be rewritten while drawing is in progress.
FPU_SHAD_SCALE	0x005F8074	Must not be rewritten while drawing is in progress.
FPU_CULL_VAL	0x005F8078	Must not be rewritten while drawing is in progress. It is strongly recommended that the value be set to a number other than '0'.
FPU_PARAM_CFG	0x005F807C	Must not be rewritten while drawing is in progress. Bit19-0 must be set to 0x7DF77 . No other settings can be used.
HALF_OFFSET	0x005F8080	Must not be rewritten while drawing is in progress. Normally, this must be set to 0x00000007.
FPU_PREP_VAL	0x005F8084	Must not be rewritten while drawing is in progress. It is strongly recommended that the value be set to a number other than '0'.
ISP_BACKGND_D	0x005F8088	Must not be rewritten while drawing is in progress.
ISP_BACKGND_T	0x005F808C	Must not be rewritten while drawing is in progress. Skip cannot be set to '0'. The BG Parameter must be allocated to tag address + PARAM_BASE.
ISP_FEED_CFG	0x005F8098	Must not be rewritten while drawing is in progress. It is strongly recommended that Cache Size for Translucency be set to the highest value. It is also recommended that Punch Through Chunk Size be set to '0x40'. When using the Half-transparent Modifier, auto sort mode must be set.
SDRAM_REFRESH	0x005F80A0	Except for BOOTROM, access is inhibited. Must be set before releasing SDRAM I/F soft reset. The product setting is 0x20.
SDRAM_ARB_CFG	0x005F80A4	Access inhibited.
SDRAM_CFG	0x005F80A8	Except for BOOTROM, access is inhibited. Must be set before releasing SDRAM I/F soft reset. The product setting is 0x15D1C951.
FOG_COL_RAM	0x005F80B0	Must not be rewritten while drawing is in progress.
FOG_COL_VERT	0x005F80B4	Must not be rewritten while drawing is in progress.
FOG_DENSITY	0x005F80B8	Must not be rewritten while drawing is in progress.
FOG_CLAMP_MAX	0x005F80BC	Must not be rewritten while drawing is in progress.
FOG_CLAMP_MIN	0x005F80C0	Must not be rewritten while drawing is in progress.
SPG_HBLANK_INT	0x005F80C8	The value of hblank_in_interrupt must be set lower than the hcount in SPG_LOAD (0x005F80D8).
SPG_VBLANK_INT	0x005F80CC	The value of line number must be set lower than the vcount in SPG_LOAD (0x005F80D8).
SPG_CONTROL	0x005F80D0	Except for bits 8, 7, 6, and 4, all other bits must be set to '0'. This register should only be written to when nothing is displayed. If rewritten when something is displayed, the image may be disrupted.
SPG_HBLINK	0x005F80D4	* See the synchronized settings table. This register should only be written to when nothing is displayed. If rewritten when something is displayed, the image may be disrupted.
SPG_LOAD	0x005F80D8	* See the synchronized settings table. This register should only be written to when nothing is displayed. If rewritten when something is displayed, the image may be disrupted.
SPG_VBLANK	0x005F80DC	* See the synchronized settings table. This register should only be written to when nothing is displayed. If rewritten when something is displayed, the image may be disrupted.
SPG_WIDTH	0x005F80E0	* See the synchronized settings table. This register should only be written to when nothing is displayed. If rewritten when something is displayed, the image may be disrupted.
TEXT_CONTROL	0x005F80E4	Bit 31-5 must be set to '0'.
VO_CONTROL	0x005F80E8	Bit 21-16 must be set to '0x16'. No other values can be set. Bit 7-4 and bit 2-0 must be set to '0'. This register should only be written to when nothing is displayed. If rewritten when something is displayed, the image may be disrupted.
VO_STARTX	0x005F80EC	* See the synchronized settings table. This register should only be written to when nothing is displayed. If rewritten when something is displayed, the image may be disrupted.
VO_STARTY	0x005F80F0	* See the synchronized settings table. This register should only be written to when nothing is displayed. If rewritten when something is displayed, the image may be disrupted.
SCALER_CTL	0x005F80F4	Must not be rewritten while drawing is in progress. When the v scale is set to a value higher than 0x400, the y size of FB_R_SIZE must be set to 1 less than the number of drawing lines to ensure that the last line will be displayed correctly.
PAL_RAM_CTRL	0x005F8108	Must not be rewritten while drawing is in progress. Must be set before Palette RAM is updated. However, setting is not necessary when the same color mode as before is used.
FB_BURSTCTRL	0x005F8110	0x00093F39 must be set. No other values can be set.
PT_ALPHA_REF	0x005F811C	Must not be rewritten while drawing is in progress.
TA_OL_BASE	0x005F8124	Must not be rewritten during TA operation.
TA_ISP_BASE	0x005F8128	Must not be rewritten during TA operation.
TA_OL_LIMIT	0x005F812C	Must not be rewritten during TA operation. When a limit occurs, 32-bytes starting at the specified base address are used. Therefore, LIMIT must not be the same as any other base address.
TA_ISP_LIMIT	0x005F8130	Must not be rewritten during TA operation. When a limit occurs, 32-bytes starting at the specified base address are used. Therefore, LIMIT must not be the same as any other base address.
TA_GLOB_TILE_CLIP	0x005F813C	Must not be rewritten during TA operation. Must be set before writing to TA_LIST_INIT.
TA_ALLOC_CTRL	0x005F8140	Must not be rewritten during TA operation. Must be set before writing to TA_LIST_INIT.
TA_LIST_INIT	0x005F8144	Must not be rewritten during TA operation. TA_GLOB_TILE_CLIP, TA_ALLOC_CTRL, and TA_NEXT_OPB_INIT must be set before writing to this register.
TA_LIST_CONT	0x005F8160	Must not be rewritten during TA operation. The TA_OL_BASE register must be up-dated when implementing continuous processing.
TA_NEXT_OPB_INIT	0x005F8164	Must not be rewritten during TA operation. Must be set before writing to TA_LIST_INIT.
FOG_TABLE	0x005F8200 | 0x005F83FD	Must not be rewritten while drawing is in progress.
PALETTE_RAM	0x005F9000 | 0x005F9FFF	Must not be rewritten while drawing is in progress.

Notes and restrictions on Drawing System Registers

(1) TA

I) During TA operation, follow the order shown below.

1. Implement TA soft reset.
2. Set TA_GLOB_TILE_CLIP, TA_ALOOC_CTRL, and TA_NEXT_OPB_INIT to the appropriate values.
3. Initialize TA by TA_LIST_INIT.
4. Send.

II) During Ch2 DMA, forcibly interrupt TA operation as follows:

1. Suspend SB Ch2 DMA.
2. Do a TA soft reset.
3. Confirm suspension of SB Ch2 DMA.
4. Suspend SH4 Ch2 DMA.
5. Implement TA soft reset once more to make sure there is no data left in the TA FIFO.

III) When using the User Tile Clip, more than 1 invisible dummy polygon must be sent immediately before changing the clip area and global parameters that change INSIDE, OUTSIDE, and DISABLE.

IV) Direct data (such as textures) cannot be sent during YUV macro block transfer.

(2) Drawing

I) End of TSP should be used for drawing complete interrupt.
Furthermore, it is strongly recommended that the End of ISP and End of Video interrupts be cleared at the same time in order to make debugging easier when an error occurs.

II) When the y scale is reduced (such as for flicker filter), the display area must be set to the drawing area-1 to ensure that the last line of the drawing area is displayed correctly.

III) An invisible opaque polygon that covers the whole screen must be registered when using half-transparent polygons with pre-sort.

IV) When modifying half-transparent and tri-linear polygons, the half-transparent sorting mode must be set to auto sort.

V) Intensity shadow volume cannot be used for polygons that use bump map texture.
However, parameter selection volume may be used.

VI) The three restrictions below must be observed when using strip buffer mode with the frame buffer.

1. Ignore the first hazard interrupt that occurs immediately after the strip buffer modeis set.
2. Make sure that the screen is divided into an even number of areas.
3. Make sure that the values of FB_X_CLIP and FB_Y_CLIP are not smaller than the screen size.

CLX BUG LIST Mar/4/99

CORE&TA

No.	PROBLEMS	Software Measure		RESTRICTIONS/MEASURES	Hardware Fix		
		Yes/No	Number		CLX2.4	CLX2.41	CLX2.42
1	VSYNC width at PAL non-interlace is 3H.	-	-	DVE corrects it to 2.5H. No problems.	No	No	No
2	In Strip Buffer mode, Hazard interupt is issued even when not rendering.	Yes	CR-6	Ignore the first Hazard interrupt. Once rendering is started, the 2nd Harzard interrupt is issued correctly.	No	No	No
3	In Strip Buffer mode, incorrect pixels will appear on upper left of the screen if Strip Buffer size is set to the number which can divide the screen by odd numbers.	Yes	CR-6	Strip Buffer size must be the number which can divide the screen by even numbers.	No	No	No
4	In Strip Buffer mode, incorrect pixels will appear at the right most side if X clipping is performed.	Yes	CR-6	In Strip Buffer mode, X clipping feature must not be used. Specify the screen x-direction size for a FB_X_CLIP register value.	No	No	No
5	The timing for User Tile Clip switch (area by Control Parameters or usage by Global Parameters) is 1 polygon (=1strip) ahead.	Yes	TA-3	Take either one of the followings as software counter measure: 1) Add a dummy polygon before the clip switching 2) Do not use User Tile Clip. Use Global Tile Clip instead.	No	No	No
6	End_Of_Video interrupt sometimes not issued.	Yes	CR-1	End_Of_TSP should be used for rendering end interrupt.	No	No	No
7	Rendering sometimes rocks up if sort mode for translucent polygon is switched for each tile.	Yes	CR-3	Take either one of the followings as software counter measure: 1) Do not switch Sort mode for each tile 2) Register Opaque polygons as background for full screen.	No	No	No
8	When Y Scaler is set greater than 0x400 and filtering is done, the result of filtering of FB output final line (32 pixel) of the last tile gets influenced by the leftmost pixel color of the line.	Yes	CR-2	Take either one of the followings as software counter measure: 1) Make the number of lines to be displayed 1 line shorter than the lines to be rendered. 2) Add a dummy final Region Array data to up-right (Y=0) of out of the screen.	No	No	No
9	Gap and/or rewirite will occur if polygon edge is negative side from the pixel center point but closer to "0".	No	-	No counter measures by software. Would be no problems after the running change.	No	No	No
10	A hung-up occurs if Non-twiddle formatted BumpMap textures are used.	Yes	restriction	BumpMap textures must be used in Twiddle format only.	No	No	No
11	Group_En bit(bit 23) within the Global Parameter cannot be valid for User_Clip bit(bit17-16).	Yes	restriction	User_Clip bit must be specified correctly for each Global Parameter.	No	No	No
12	Texture data flickers (VQ is remarkable). Also it may destroy data within texture memory). It is because drive Tr within the F091is lack of ability.	No	-	No counter measures by software. In CLX2.41, clump the one which is SDIF block In CLX2.5, clump the one which is full block.	No		Yes
13	End Of Render(End Of TSP) is not output if Y Scaler is modified & rendered as follows: Scale-up -> Scale-down, or Non-scale -> Scale-down.	Yes	CR-7	When Y Scaler is modified and rendered like noted left, perform CORE Reset between two times of rendering.	No	No	No

REGISTER

No.	PROBLEMS	Software Measure		RESTRICTIONS/MEASURES	Hardware Fix		
		Yes/No	Number		CLX2.4	CLX2.41	CLX2.42
1	Does not work correctly even if the LSB of fb_stripsize in FB_R_CTRL register (0x005F8044) is set to 1.	Yes	restriction	Strip Buffer size is limited at the unit of 32lines.	No	No	No

SYSTEM	Resolution	FB_R_CTRL [vclk_div]	SPG_LOAD	SPG_HBLANK	SPG_VBLANK	SPG_WIDTH	SPG_CONTROL	VO_STARTX	VO_STARTY	VO_CONTROL
VGA	640x480	1	0x020C0359	0x007E0345	0x00280208	0x03F1933F	0x00000100	0x000000A8	0x00280028	0x00160000
NTSC-NI	320x240	0	0x01060359	0x007E0345	0x00120102	0x03F1933F	0x00000140	0x000000A4	0x00120011	0x00160100
	640x240	0	0x01060359	0x007E0345	0x00120102	0x03F1933F	0x00000140	0x000000A4	0x00120011	0x00160000
NTSC-I	320x480	0	0x020C0359	0x007E0345	0x00240204	0x07D6C63F	0x00000150	0x000000A4	0x00120012	0x00160100
	640x480	0	0x020C0359	0x007E0345	0x00240204	0x07D6C63F	0x00000150	0x000000A4	0x00120012	0x00160000
PAL-NI	320x240	0	0x0138035F	0x008D034B	0x002C026C	0x07F1F53F	0x00000180	0x000000AE	0x002E002E	0x00160100
	640x240	0	0x0138035F	0x008D034B	0x002C026C	0x07F1F53F	0x00000180	0x000000AE	0x002E002E	0x00160000
PAL-I	320x480	0	0x0270035F	0x008D034B	0x002C026C	0x07D6A53F	0x00000190	0x000000AE	0x002E002D	0x00160100
	640x480	0	0x0270035F	0x008D034B	0x002C026C	0x07D6A53F	0x00000190	0x000000AE	0x002E002D	0x00160000