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SEGA SATURN

SCU Final Specifications: Precautions

(Version 1)

Doc. # ST-210-110194

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REFERENCES

In translating/creating this document, certain technical words and/or phrases were interpreted with the assistance of the technical literature listed below.

1. *KenKyusha New Japanese-English Dictionary*
   1974 Edition

2. *Nelson's Japanese-English Character Dictionary*
   2nd revised version

3. *Microsoft Computer Dictionary*

4. *Japanese-English Computer Terms Dictionary*
   Nichigai Associates
   4th version

0. Introduction

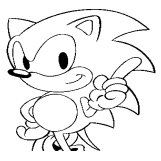
This document contains the final specifications and items of note about the SEGA Saturn SCU. Since it consists of material which is not included in the previous manual, be sure to check the contents against this newest manual.

[Revision History]

Sept. 20, 1994	Provisional version issued
Oct. 11, 1994	2nd provisional version (added No. 35 and No. 36)
Oct. 16, 1994	1st version issued (revised No. 35 and No. 36)

1. SCU Final Specifications List

No. 01	Write to the A-Bus by SCU-DMA is prohibited.
No. 02	Read from the VDP2 area by SC-DMA is prohibited.
No. 03	VDP1 register write access must be in word units (2 bytes).
No. 04	Do not use SCU-DMA to WORK RAM-L (Caution).
No. 05	Must use the cache through address to access the SCU register .
No. 06	Reads and writes to unused areas (address 25FE00AC$_H$) are prohibited.
No. 07	Writes to interrupt status register (25FE00A4H) are prohibited.
No. 08	Access to A-Bus and B-Bus from the CPU during DMA operation of A-Bus $\leftrightarrow$ B-Bus is prohibited.
No. 09	Setting the A-Bus preread significant bit is prohibited.
No. 10	A-Bus interrupt acknowledge register address change (address 25FE00A8$_H$).
No. 11	A-Bus set register write restriction (addresses 25FE00B0$_H$ and 25FE00B4$_H$).
No. 12	A-Bus $\leftarrow \rightarrow$ B-Bus SCU-DMA start standby when CPU writes to the A-Bus and B-Bus.
No. 13	Delete the DMA status register (addresses 25FE0070$_H$ ~ 25FE007C$_H$).
No. 14	Delete the DMA forced quit register function (address 25FE0060$_H$).
No. 15	Read of DMA transfer register transfer byte number is prohibited (write only).
No. 16	Restrictions by the address accessing the DMA read address add value.
No. 17	Value of the address add value bit when setting the DMA read address update bit.
No. 18	Restrictions by the address accessing the DMA write address add value.
No. 19	Value of the address add value bit when setting the DMA write address update bit.
No. 20	2 channels can be used for simultaneous use of DMA.
No. 21	DMA activation method specification change.
No. 22	Specification when DMA start trigger occurs during DMA execution.
No. 23	Writing to the register of the corresponding level while activating DMA is prohibited.
No. 24	DMA illegal interrupt does not occur during DMA execution in the indirect mode.
No. 25	DMA indirect mode table specification change.
No. 26	Clears the program end interrupt flag when starting DSP.
No. 27	Address add value restriction when transferring from the DSP DMA command B-Bus to the DSP Data RAM.
No. 28	When debugging with ICE, starting DMA operation is delayed if a BREAK is performed.
No. 29	Must be the BREQ enable condition when debugging in ICE.
No. 30	Caution when using the Timer 0 compare register (address 25FE0090$_H$).
No. 31	Caution when using the Timer 1 set data register (address 25FE0094$_H$).
No. 32	Caution during read access of A-Bus and B-Bus areas (200000$_H$ ~ 5FFFFFF$_H$).
No. 33	A-Bus refresh initial value when Power ON is reset (address 25FE00B8$_H$).
No. 34	Initial value of the SDRAM selection bit (address 25FE00C4$_H$).
No. 35	Start of DMA level 2 is prohibited during execution of DMA level 1.
No. 36	Caution when reading the DSP program control port (address 25FE0080$_H$)



2. SCU Final Specification Reference Items

1. Items concerning the entire DMA .	
Item No.	01, 02, 04, 08, 12, 13, 14, 15, 16, 17, 18, 19, 20, 21, 22, 23, 24, 25, 26, 27, 28, 29 and 3

2. DMA indirect mode specific items.	
Item No.	24 and 25

3. Items relating to the DSP.	
Item No.	16, 20, 26, 27 and 36

4. Items regarding external areas (A-Bus).	
Item No.	01, 08, 09, 10, 11, 12, 17, 18, 19 and 32

5. Items regarding B-Bus areas (VDP1, VDP2, SCSP).	
Item No.	02, 03, 08, 12, 17, 18, 19 and 32

6. Items regarding interrupt.	
Item No.	07, 30 and 31

7. SCU register specification change items.	
Item No.	07, 09, 10, 11, 13, 14, 15, 23 and 24

8. Items relating to debugging.	
Item No.	28 and 29

3. SCU Final Specification Contents

No. 01	Write to the A-Bus by the SCU-DMA is prohibited.
Write to the A-Bus by SCU-DMA cannot be used.	

No. 02	Read from the VDP2 area by SCU-DMA is prohibited.
Read by SCU-DMA from the VDP2 area cannot be used.	

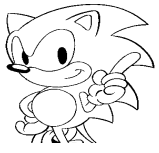
No. 03	VDP1 register write access must be in word units (2 bytes).
VDP1 register write access must be in word (2 byte) units. Access in long word (4 bytes) byte units is prohibited. VDP1 read access can be in byte and long word units.	

No. 04	Use of SCU-DMA to WORK RAM-L is not able (Caution).
Work RAM-H (SDRAM: 1 Mbyte) is the only Work RAM that can be used with SCU-DMA. Work RAM-L (DRAM: 1 Mbyte) cannot be used.	

No. 05	Access to the SCU register must use the cache through address.
Register access to the SCU must be done by the cache-through address. This is because a register in which read is prohibited may be accessed if the cache address is used since the CPU runs in the following way when the cache is full. • When 0H address data is read by the cache address 4H address read→ 8H address read→ CH address read→ 0H address read→ cache register • When 4H address data is read by the cache address 8H address read→ CH address read→ 0H address read→ 4H address read→ cache register • When 8H address data is read by the cache address CH address read→ 0H address read→ 4H address read→ 8H address read→ cache register • When CH address data is read by the cache address 0H address read→ 4H address read→ 8H address read→ CH address read→ cache register	

No. 06	Read and write to unused areas (address 25FE00AC etc.) is prohibited.
Reading and writing to unused areas are prohibited. Reading and writing to address 25FE00AC is especially prohibited.	

No. 07	Write to the interrupt status register (25FE00A4) is prohibited.
When writing to the interrupt status register, the bit used to create interrupt may not be active. Therefore, writing to the interrupt status register is prohibited.	



No. 08	Access to A-Bus and B-Bus from the CPU during DMA operation of A-Bus ↔ B-Bus is prohibited.
During the DMA operation of A-Bus to B-Bus and B-Bus to A-Bus, access from the CPU to the A-Bus and B-Bus is prohibited. Refresh is not generated for SDRAM while waiting and may hang up.	

No. 09	Setting the A-Bus preread significant bit is prohibited.
The A-Bus preread function was deleted. The following register bits listed in the 2nd version manual (May 31, 1994) must be set to 0. 1. A-Bus set register [CS0, 1 space] (address: 25FE00B0H, register: ASR0) → [bit 31] and [bit 15] must be set to 0. 2. A-Bus set register [CS2, reserved space] (address: 25FE00B4H, register: ASR1) → [bit 31] and [bit 15] must be set to 0.	

No. 10	Address change of the A-Bus interrupt acknowledge register (address 25FE00A8H)
The address of the A-Bus interrupt acknowledge register is changed to 25FE00A8H. The contents of change is reflected in the 2nd version manual (May 31, 1994).	

No. 11	A-Bus set register write restriction (addresses 25FE00B0H and 25FE00B4H).
The A-Bus set register enables to write to the A-Bus only when not accessing. Write after completing read of the A-Bus (dummy).	

No. 12	A-Bus ← → B-Bus SCU-DMA start standby when the CPU writes to the A-Bus and B-Bus.
The write process by the CPU to the A-Bus and B-Bus is higher in priority than the SCU-DMA start between the A-Bus and B-Bus. For example, while continuous write is performed by the CPU to VDP (B-Bus), SCU-DMA does not start until continuous write ends even if SCU-DMA initial activation for VDP2 (B-Bus) from the A-Bus. However, while starting SCU-DMA, CPU access to A-Bus and B-Bus is on standby.	

No. 13	Delete the DMA status register (addresses 25FE0070H ~ 25FE007CH).
The function that returns the address set value of DMA while stopped and the status of levels 0, 1, 2 been deleted. Part of the specification change is reflected in the 2nd version manual (May 31, 1994) (The DMA read address, write address, and transfer byte number while stopped were deleted.)	

No. 14	Delete the DMA forced quit register function. (Address 25FE0060H)
DMA forced quit register functions was deleted. Writing to this register is prohibited.	

No. 15	Read of DMA transfer register transfer byte is prohibited (write only).

The value reading the number of transfer bytes number of the DMA transfer register is not guarantee
This register cannot be read. This is a write-only register. (address, level 0, 25FE0008H: D0C, level 1,
25FE0028H : D1C, level 2, 25FE0048H : D2C).

No. 16	Restrictions by the address accessing the DMA read address add value.

The value that can be set in the read address add value changes by the address that is to be acces
This applies to DMA commands of the DSP.

External area 4 (A-Bus I/O area)	→	Able to set 0B and 1B.
Other	→	Able to set 1B only.

(Address: level 0, 25FE000CH: D0RA, level 1, 25FE002CH: D1RA, level 2, 25FE004CH: D2RA)

No. 17	Value of the address add value bit when setting the DMA read address update bit.

When the read address update bit*1 is 1, the read address add value bit*2 must be 1.

*1 Read address update bit
Address: level 0, 25FE0014H: D0RUP, level 1, 25FE0034H: D1RUP, level 2, 25FE0054H: D2RUP

*2 Read address add value bit
Address: level 0, 25FE000CH: D0RA, level 1, 25FE002CH: D1RA, level 2, 25FE004CH: D2RA

No. 18	Restrictions by the address accessing the DMA write address add value.

Values that can be set in the write address add value change according to the address that is access
This applies to DMA commands of the DSP.

WORK RAM-H	→	Able to set 010B
External area 1 ~ 3	→	Able to set 010B
External area 4 (A-Bus I/O area)	→	Able to set 000B and 010B.
VDP1, VDP2, SCSP	→	All settings are possible.

(Address: level 0, 25FE000CH: D0WA, level 1, 25FE002CH: D1WA, level 2, 25FE004CH: D2WA)

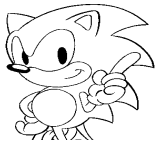
No. 19	Value of the address add value bit when setting the DMA write address refresh bit.

When the write address update bit*1 is 1, the write address add value bit*2 must be set by the bus space
to be accessed as shown below.

External area 1 ~ 4 (A-Bus)	→	Able to set 010B
VDP1, VDP2, and SCSP (B-Bus)	→	Able to set 001B
Work RAM-H ((C-Bus)	→	Able to set 010B

*1 Write address update bit
Address: level 0, 25FE0014H: D0WUP, level 1, 25FE0034H: D1WUP, level 2, 25FE0054H: D2WUP

*2 Write address add value bit
Address: level 0, 25FE000CH: D0WA, level 1, 25FE002CH: D1WA, level 2, 25FE004CH: D2WA



No. 20	2 channels are available for the simultaneous use of DMA.

Up to 2 channels can be used concurrently which guarantee the priority order of DMA . If 3 channels used concurrently, the priority order is ignored. (The DSP DMA command is also counted as 1 chann

No. 21	DMA activation method specification changes.

The start method of DMA has been changed and a DMA enable bit has been provided separately.

Start Factor	DMA Start Conditions
0 0 0	Enable bit = 1 AND V-BLANK-IN
001	Enable bit = 1 AND V-BLANK-OUT
010	Enable bit = 1 AND H-BLANK-IN
011	Enable bit = 1 AND TIMER 0
100	Enable bit = 1 AND TIMER 1
101	Enable bit = 1 AND SCSP Request
110	Enable bit = 1 AND Sprite draw end
111	Enable bit = 1 AND DMA Start Bit = 1

These changes are reflected in the 2nd version manual (May 31, 1994.)

No. 22	Specification when a DMA start trigger occurred during DMA execution.

If a DMA start trigger occurs while DMA is being executed, and it holds the trigger, then execute activation after DMA ends. For example, when set so that DMA starts at H-Blank, operation becomes unstable if the set data size is larger than the size enabling transfer within 1 line (until the next H-blank When such DMA start is executed in this way, please note the transfer data size. The trigger hold hol only for 1 time.

No. 23	Writing to the register of the corresponding level while starting DMA is prohibited.

Rewriting the contents of DMA mode, address update, activation factor selection register*1 and DMA set register*2 is not allowed during DMA activation at this level. Hang up occurs if rewritten.

*1 DMA mode, address update, start factor select register
Address: Level 0, 25FE0014H, level 1 25FE0034H, level 2 25FE0054H

*2 DMA set register
Address: Level 0, 25FE000CH, level 1 25FE002CH, level 2 25FE004CH

No. 24	DMA illegal interrupt does not occur during DMA execution in the indirect mode.

The DMA illegal interrupt status bit [bit 12] of the DMA status register (address 25FE0040H) does not occur in the indirect mode while DMA is executing. When DMA is used in the indirect mode, do not re to the DMA illegal interrupt status bit.

No. 25	DMA indirect mode table specification change.

Tables of DMA indirect mode have been changed as shown below.

[Points of Change]

1. The 4 long word configuration has been changed to a 3 long word configuration.
2. The write address and read address have been reversed.
3. The table address (m value in the table below) must place the beginning address in 32, 64 128, 2 512,1024, · · ·byte boundaries according to table size (n X 12 bytes). An example is shown below
   - Table size is 24 bytes or less → place at the start address 32 byte boundary.
   - Table size is 252 bytes or less → place at the start address 256 byte boundary.
   - Table size is 1020 bytes or less→ place at the start address 1024 byte boundary.
4. A 1 must be set to the 31st bit of the read address of the final address (n th).

Address is set in the write → m
address register

m	first transfer byte number
m + 4	first write address
m + 8	first read address
	. . .
	nth transfer byte number
	nth write address
	nth read address

Set 1 in the 31st bit of the nth read→ address

(Address: level 0, 25FE0004H, level 1, 25FE0024H, level 2, 25FE0044H)

No. 26	Clears the program end interrupt flag when starting DSP.

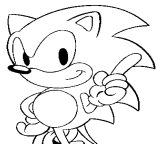
Be sure the program end interrupt flag [bit 18 : E] of the DSP program control port (address 25FE0008H) is 0 when starting DSP. If the flag is 1, DSP program end interrupt does not occur even if the DSP program ends by the ENDI command.

No. 27	Address add value restriction when transferring from the DMA command B-Bus of the DSP to the Data RAM of the DSP.

The address add value must be 0 when transferring from the B-Bus to the Data RAM of DSP with the DSP DMA command (DMA and DMAH).

No. 28	When debugging in ICE, starting DMA operation is delayed if a BREAK is performed.

SCU DMA must be executed by the CPU. If there is a break while debugging in ICE, the start of the SCU-DMA operation will be delayed. Operation of the SCU-DMA is normally performed when the ICE execution condition is the parallel mode (prompt is the # condition).



No. 29	Must be the BREQ enable condition when debugging in ICE.

When SCU-DMA is used in ICE, the input condition of the EXECUTION_MODE (EM) command BREQ (bus right request) signal must be E (always enabled). Changing the E7000 system of ICE is unnecessary because BREQ is E by default.

No. 30	Caution when using the Timer 0 compare register (address 25FE0090H)

It is possible to set up to 10 bits of data, but if data that does not exist, interrupt won't occur . Be sure set a value within a range that can be used. In case of an NTSC non-interface (1 screen 263 lines, effective screen 224 lines), for example, interrupt will occur as follows:

T0C9–0 = 1 → Occurs at the start of H-Blank-IN just before the first 1 line of the effective scree
T0C9–0 = 2 → Occurs at the start of H-Blank-IN just before the first 2 line of the effective scree
T0C9–0 = 224 → Occurs at the start of H-Blank-IN just before the last 1 line of the effective scree
T0C9–0 = 225 → Occurs at the start of H-Blank-IN just after the effective screen ends.
T0C9–0 = 263 → Occurs at the start of H-Blank-IN just 1 line before the beginning of the effective screen.
T0C9–0 = 264 ~ 1023 → Interrupt does not occur.
T0C9–0 = 0 → Interrupt occurs with the same timing as V-Blank-OUT.

No. 31	Caution when using the Timer 1 set data register (address 25FE0094H)

Loading the value of Timer 1 set data register to Timer 1 occurs "when Timer 1 is stopped and H-Blan occurs." If data larger than the count number of 1 line is set to the Timer 1 set data register, Timer 1 interrupt no longer occurs for each line.

[Count Number Range]

For 1 line 320 dots: 1 ~ 1AAH
For 352 dots 1 ~ 1C6H
For 424 dots 1 ~ D3H
For 426 dots 1 ~ D4H

(Be aware that this becomes 512 when a count number of 0 is specified)

No. 32	Caution during read access of A-Bus and B-Bus areas (2000000H ~ 5FFFFFFH)

The internal CPU operation and external operation are different for read access of the A-Bus and B-B areas (2000000H ~ 5FFFFFFH). Even for byte or word (2 bytes) read access from the SH2, the externa is accessed by long word (4 bytes) units. When performing byte unit read of a continuous area in the Bus and B-Bus areas, more process time than for byte unit write is required. Internal operations and external operations are the same for write access. (External access becomes byte access when accessed in byte units.)

No. 33	A-Bus refresh initial value when Power ON is reset (address 25FE00B8H)
The initial value of the A-Bus refresh output effective bit when resetting power on is changed to an effective condition (ARFEN = 1). This bit should not be changed by the user.	

No. 34	Initial value of the SDRAM selection bit (address 25FE00C4H)
The SDRAM selection bit becomes 2 Mbits X 2 (RSEL = 0) by resetting the power on. Reset to RSEL 1 and change to 4 Mbits X 2. This change in setting is done within the Boot ROM and requires no change by the user.	

No. 35	Start of DMA level 2 is prohibited during execution of DMA level 1.
A malfunction can occur when DMA level 2 is activated while starting DMA at level 1. Do not start DM level 2 while DMA level 1 is activated.	

No. 36	Caution when reading the DSP program control port (address 25FE0080H)
Be aware that the following phenomenon occurs when reading the DSP program control port. 1. V-Flag (overflow flag) is cleared away. A check of the V-Flag cannot be done while executing DSP. 2. The DSP end interrupt factor may not occur. Because the DSP end interrupt may not occur when the program end interrupt flag is read while DSP is being executed, please do not read this address for the program obtained by DSP end interrupt.